WHAT IS CLAIMED IS:

1. A voltage controlled oscillator (VCO) comprising a ring oscillator having an input, an output, an odd number M of complementary metal oxide semiconductor (CMOS) inverters series coupled between the input and output, a feedback connection between the input and output, and a number K of voltage controlled feedforward (FF) stages, each of the K FF stages coupled in parallel with K groups of an odd number of G sequential CMOS inverters selected from the M CMOS inverters, each of the K FF stages having a plurality P channel metal oxide silicon transistors (PFETs) and a plurality of N channel metal oxide silicon transistors (NFETs), at least one of the PFETs having a first isolated region of semiconductor material (body) connected to a first body terminal, and at least one of the NFETs having a second isolated body connected to a second body terminal, wherein the K FF stages are controlled by first and second control voltages coupled to the first and second body terminals respectively.

2. The VCO of claim 1, wherein each of the K FF stages comprises a CMOS inverter stage coupled in series with a transfer gate stage having a parallel connection of a first PFET and a first NFET.

3. The VCO of claim 2, wherein the first PFET of the transfer gate stage has a body terminal coupled to the first control voltage and the NFET of the transfer gate a body terminal coupled to the second control voltage.

4. The VCO of claim 1, wherein the second control voltage is derived from the first control voltage such that the first and the second control voltages have a same nominal value and opposite slopes when modified.

5. The VCO of claim 2, wherein each of the CMOS inverters in the K FF stages comprise a second PFET and a second NFET coupled in series, wherein the second PFET of at least one of the CMOS inverters has a body terminal coupled to the first control voltage and the second NFET of the at least one of the CMOS inverters has a body terminal coupled to the second control voltage.

6. The VCO of claim 3, wherein each of M CMOS inverters comprise a third PFET and a third NFET, wherein the third PFET of at least one of the M CMOS inverters has a body terminal coupled to the first control voltage and the third NFET of the at least one of the M CMOS inverters has a body terminal coupled to the second control voltage.

7. The VCO of claim 5, wherein each of M CMOS inverters comprise a third PFET and a third NFET, wherein the third PFET of at least one of the M CMOS inverters has a body terminal coupled to the first control voltage and the third NFET of the at least one of the M CMOS inverters has a body terminal coupled to the second control voltage.

8. The VCO of claim 2 wherein each of the CMOS inverters in the K FF stages comprise a second PFET and a second NFET coupled in series, wherein the second PFET of at least one of the CMOS inverters has a body terminal coupled to the first control voltage by a first clamping circuit preventing a body diode coupled to the body terminal of the second PFET from being forward biased and the second NFET of the at least one of the CMOS inverters has a body terminal coupled to the second control voltage by a second clamping circuit preventing a body diode coupled to the body terminal of the second NFET from being forward biased.

9. The VCO of claim 3, wherein each of M CMOS inverters comprise a second PFET and a second NFET coupled in series, wherein the second PFET of at least one of the CMOS inverters has a body terminal coupled to the first control voltage by a first clamping circuit preventing a body diode coupled to the body terminal of the second PFET from being forward biased and the second NFET of the at least one of the CMOS inverters has a body terminal coupled to the second control voltage by a second clamping circuit preventing a body diode coupled to the body terminal of the second NFET from being forward biased.

10. The VCO of claim 8, wherein the first clamping circuit comprises a clamping PFET having a body terminal coupled to the source of the second PFET, a gate coupled to ground potential, a drain coupled to the body terminal of the second PFET and a source coupled to the first control voltage and the second clamping circuit comprises a clamping NFET having a body terminal coupled to the source of the second NFET, a gate coupled to the positive power supply voltage, a drain coupled to the body terminal of the second NFET and a source coupled to the first control voltage.

11. The VCO of claim 9, wherein the first clamping circuit comprises a clamping PFET having a body terminal coupled to the source of the second PFET, a gate coupled to ground potential, a drain coupled to the body terminal of the second PFET and a source coupled to the first control voltage and the second clamping circuit comprises a clamping NFET having a body terminal coupled to the source of the second NFET, a gate coupled to the positive power supply voltage, a drain coupled to the body terminal of the second NFET and a source coupled to the first control voltage.

12. The VCO of claim 1, wherein K is equal to M.

13. A phase locked loop (PLL) circuit for generating an output clock signal with a frequency that is a multiple number N times the frequency of a reference clock signal, comprising:

a voltage controlled oscillator (VCO) generating the output clock signal with a frequency modified in response to a control voltage;

a frequency divider for frequency dividing the output clock signal by N, generating a frequency divided clock signal;

a phase frequency detector for comparing the frequency divided clock signal to the reference clock signal and generating a phase/frequency error signal; and

circuitry for converting the phase/frequency error signal to the control voltage, wherein the VCO is a ring oscillator having an input, an output, an odd number M of complementary metal oxide semiconductor (CMOS) inverters series coupled between the input and output, a feedback connection between the input and output, and a number K of voltage controlled feedforward (FF) stages, each of the K FF stages coupled in parallel with K groups of an odd number of G sequential CMOS inverters selected from the M CMOS inverters, each of the K FF stages having a plurality P channel metal oxide silicon transistors (PFETs) and a plurality of N channel metal oxide silicon transistors (NFETs), at least one of the PFETs having a first isolated region of semiconductor material (body) connected to a first body terminal, and at least one of the NFETs having a second isolated body connected to a second body terminal, wherein the K FF stages are controlled by first and second control voltages coupled to the first and second body terminals respectively.

14. The PLL circuit of claim 13, wherein each of the K FF stages comprise a CMOS inverter stage coupled in series with a transfer gate stage having a parallel connection of a first PFET and a first NFET.

15. The PLL circuit of claim 14, wherein the first PFET of the transfer gate stage has a body terminal coupled to the first control voltage and the NFET of the transfer gate a body terminal coupled to the second control voltage.

16. The PLL circuit of claim 13, wherein the second control voltage is derived from the first control voltage such that the first and the second control voltages have a same nominal value and opposite slopes when modified.

17. The PLL circuit of claim 14, wherein each of the CMOS inverters in the K FF stages comprise a second PFET and a second NFET coupled in series, wherein the second PFET of at least one of the CMOS inverters has a body terminal coupled to the first control voltage and the second NFET of the at least one of the CMOS inverters has a body terminal coupled to the second control voltage.

18. The PLL circuit of claim 15, wherein each of M CMOS inverters comprise a third PFET and a third NFET, wherein the third PFET of at least one of the M CMOS inverters has a body terminal coupled to the first control voltage and the third NFET of the at least one of the M CMOS inverters has a body terminal coupled to the second control voltage.

19. The PLL circuit of claim 17, wherein each of M CMOS inverters comprises a third PFET and a third NFET, wherein the third PFET of at least one of the M CMOS inverters has a body terminal coupled to the first control voltage and the third NFET of the at least one of the M CMOS inverters has a body terminal coupled to the second control voltage.

20. The PLL circuit of claim 14, wherein each of the CMOS inverters in the K FF stages comprise a second PFET and a second NFET coupled in series, wherein the

second PFET of at least one of the CMOS inverters has a body terminal coupled to the first control voltage by a first clamping circuit preventing a body diode coupled to the body terminal of the second PFET from being forward biased and the second NFET of the at least one of the CMOS inverters has a body terminal coupled to the second control voltage by a second clamping circuit preventing a body diode coupled to the body terminal of the second NFET from being forward biased.

21. The PLL circuit of claim 15, wherein each of M CMOS inverters comprise a second PFET and a second NFET coupled in series, wherein the second PFET of at least one of the CMOS inverters has a body terminal coupled to the first control voltage by a first clamping circuit preventing a body diode coupled to the body terminal of the second PFET from being forward biased and the second NFET of the at least one of the CMOS inverters has a body terminal coupled to the second control voltage by a second clamping circuit preventing a body diode coupled to the body terminal of the second NFET from being forward biased.

22. The PLL circuit of claim 20, wherein the first clamping circuit comprises a clamping PFET having a body terminal coupled to the source of the second PFET, a gate coupled to ground potential, a drain coupled to the body terminal of the second PFET and a source coupled to the first control voltage and the second clamping circuit comprises a clamping NFET having a body terminal coupled to the source of the second NFET, a gate coupled to the positive power supply voltage, a drain coupled to the body terminal of the second NFET and a source coupled to the first control voltage.

23. The PLL circuit of claim 21, wherein the first clamping circuit comprises a clamping PFET having a body terminal coupled to the source of the second PFET, a gate coupled to ground potential, a drain coupled to the body terminal of the second PFET and a source coupled to the first control voltage and the second clamping

circuit comprises a clamping NFET having a body terminal coupled to the source of the second NFET, a gate coupled to the positive power supply voltage, a drain coupled to the body terminal of the second NFET and a source coupled to the first control voltage.

24. The PLL circuit of claim 13, wherein K is equal to M.